

PATENTS
Customer No.: 48510

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: McGINNIS, Darrell S)	Confirmation No.: 2760
)	
Patent No.:)	Group Art Unit: 2116
)	
Serial No.: 10/748836)	Examiner: YANCHUS, P. III
)	
Filed: 31 DECEMBER 2003)	Atty. Docket No.: INTEL5
)	
Title: System And Method For Scalable Clock Gearing Mechanism)	Assignee: INTEL Corporation

In accordance with 37 C.F.R. § 1.8, I certify that this correspondence is being transmitted to the Commissioner for Patents, MAIL STOP AMENDMENT, P.O. Box 1450, Alexandria, VA 22313 via the USPTO's EFS-Web Electronic Filing System on 31 MAY 2007.

/jameshuntyanceyjr53809/
James Hunt Yancey, Jr., USPTO Reg. No. 53,809

COMBINED POWER OF ATTORNEY SUBMISSION & 37 CFR § 3.73(b) STATEMENT

**Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

Dear Honorable Sir:

The undersigned representative for the Assignee of record of the above-listed patent application (INTEL Corporation) submits this power of attorney submission on behalf of INTEL Corporation. By this submission, INTEL Corporation revokes all previously granted Power of Attorneys for this application and Appoints the Practitioners associated with Customer Number 48510 to prosecute this patent application before the USPTO. As such, the undersigned respectfully requests that the USPTO's records be updated to associate this application with Customer Number 48510 to reflect this new Power of Attorney submission.

I. Express Power of Attorney Revocation & Appointment

I, Martha Peralez, revoke all previous powers of attorney given in the above-identified application. I appoint the practitioners associated with Customer Number 48510 to prosecute the above-identified application and those listed in the attached Schedule A. I also request the correspondence address for the above-identified application be changed to the address associated with Customer Number 48510.

SIGNATURE: *Martha Peralez* DATE: 5/25/07

NAME: MARTHA PERALEZ
TITLE: Administrator of Patents, INTEL Corporation
TELEPHONE: 408-765-4094

II. Statement Under 37 CFR 3.73(b)

INTEL Corporation states that is the Assignee of record for the above-listed patent or patent application by virtue of an Assignment recorded with the Assignment Branch from the inventor(s) of the patent or patent application identified above. The recordation information (Reel/Frame Number) associated with this patent application is shown in the attached Schedule A. The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

SIGNATURE: *Martha Peralez* DATE: 5/25/07

NAME: MARTHA PERALEZ
TITLE: Administrator of Patents, INTEL Corporation
TELEPHONE: 408-765-4094

CONCLUSION

The undersigned submits this *COMBINED POWER OF ATTORNEY SUBMISSION & 37 CFR § 3.73(b) STATEMENT* to appoint practitioners associated with Customer Number 48510 with this patent application as listed in Schedule A. Should USPTO personnel have any questions regarding this submission, please contact Hunter Yancey at 404-885-3696.

Respectfully submitted,

TROUTMAN SANDERS LLP

/jameshuntyanceyjr53809/
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SCHEDULE A

(Submitted With Combined Power of Attorney Submission & 37 CFR § 3.73 Statement)

	Application Serial No.	Patent No. (If Issued)	Attorney Docket No.	Assignment Recordation Reel/Frame No.	Title
1.	10/749,935	7,103,746	INTEL1	015450/0489	A Method Of Sparing Memory Devices Containing Pinned Memory
2.	10/749,924	7,177,989	INTEL2	015450/0606	Retry Of A Device Read Transaction
3.	10/749,467	6,956,775	INTEL3	015506/0676	Write Pointer Error Recovery
4.	10/749,464	7,133,960	INTEL4	015450/0486	Logical To Physical Address Mapping Of Chip Selects
5.	10/748836		INTEL5	015344/0383	System And Method For Scalable Clock Gearing Mechanism
6.	10/883,469		INTEL6	015441/0465	Method And Apparatus For Improved Pumping Medium For Electro-Osmotic Pumps
7.	10/883,466		INTEL7	015836/0255	Method For Manufacturing Porous Silicon
8.	10/814,212	7,023,089	INTEL8	014857/0041	Low Temperature Packaging Apparatus And Method
9.	10/903,694		INTEL9	015643/0464	Apparatuses And Methods For Improving Ball-Grid-Array Solder Joint Reliability
10.	10/749,465		INTEL13	015427/0529	Onboard Memory Buffer For Data Manipulation Operations
11.	10/747,824	7,001,782	INTEL16	014855/0537	Method And Apparatus For Filling Interlayer Vias On Ferroelectric Polymer Substrates
12.	10/713,718	7,127,584	INTEL17	015237/0400	System And Method For Dynamic Rank Specific Timing Adjustments For Double Data Rate (DDR) Components
13.	10/881,691		INTEL18	015837/0941	Low Power Consumption OLED Material For Display Applications

	Application Serial No.	Patent No. (If Issued)	Attorney Docket No.	Assignment Recordation Reel/Frame No.	Title
14.	10/748,109		INTEL19	015311/0082	Integrated Biometric User Authentication With Wireless Networking Device
15.	10/746,886		INTEL20	015397/0219	Automatic Network Connectivity With Power Conservation
16.	10/746,884		INTEL21	015303/0987	Application Control Registry System And Method
17.	10/749,943		INTEL22	015455/0938	System And Method For Sequencing Multiple Write State Machines
18.	10/749,934		INTEL23	015502/0647	Integrated Circuit Inductor Component
19.	10/749,466	7,159,091	INTEL25	015431/0815	Dynamic Relocation Of Execute In Place Applications
20.	10/750,364	7,200,708	INTEL26	014873/0298	Apparatus And Methods For Storing Data Which Self-Compensate For Erase Performance Degradation
21.	10/749,135		INTEL27	015527/0151	System And Method For Monitoring And Managing Connection Manager Activity
22.	10/750,367		INTEL28	015500/0470	OLED Backlight For A Liquid Crystal Display (LCD)
23.	10/820,648	7,106,147	INTEL29	014844/0585	Apparatus, System, And Method For High Frequency Signal Distribution
24.	10/814,027		INTEL30	014696/0531	Memory Programming Devices
25.	10/861,138	7,148,725	INTEL31	014856/0479	Voltage Clamp
26.	10/830,230	7,185,219	INTEL32	015261/0659	System And Method For Clock Phase Recovery
27.	10/845,019		INTEL33	015335/0299	Ability To Scale Hard Disk Password Mechanism
28.	10/930,200		INTEL34	015765/0302	Voltage Regulator